MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

EEE4186 - VLSI SYSTEM DESIGN AND MODELING TECHNIQUE

(EE, TE)

12 MARCH 2020
9:00 AM – 11:00 AM
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **5 pages** including cover page with **4 Questions** only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is the same.

3. Please print all your answers in the answer Booklet provided.

4. **A VHDL model** means an entity-architecture pair, plus any extra codes that might be necessary for them to work properly (library, use, etc.)

5. When names (of entities, architectures, signals, etc.) are not specified, you may use any suitable and valid name.

Question 1

(a) Write the characteristic equation, F of the circuit shown in Figure Q1.

[2 marks]

(b) Create the VHDL code for the circuit shown in Figure Q1 using the characteristic equation computed in part(a). Use entity name: *mux4to1* and architecture name: *mux4to1_arch.*

[9 marks]

(c) Write the **architecture** code for the circuit shown in Figure Q1 using **structural** VHDL code by the instantiate ***components*** *or4*, *and3* and *inv*. Use the architecture name: *mux4to1_arch*, and the signals *sig1*, *sig2*, *sig3*, *sig4*, *s1b* and *s2b* shown in Figure Q1.

[14 marks]

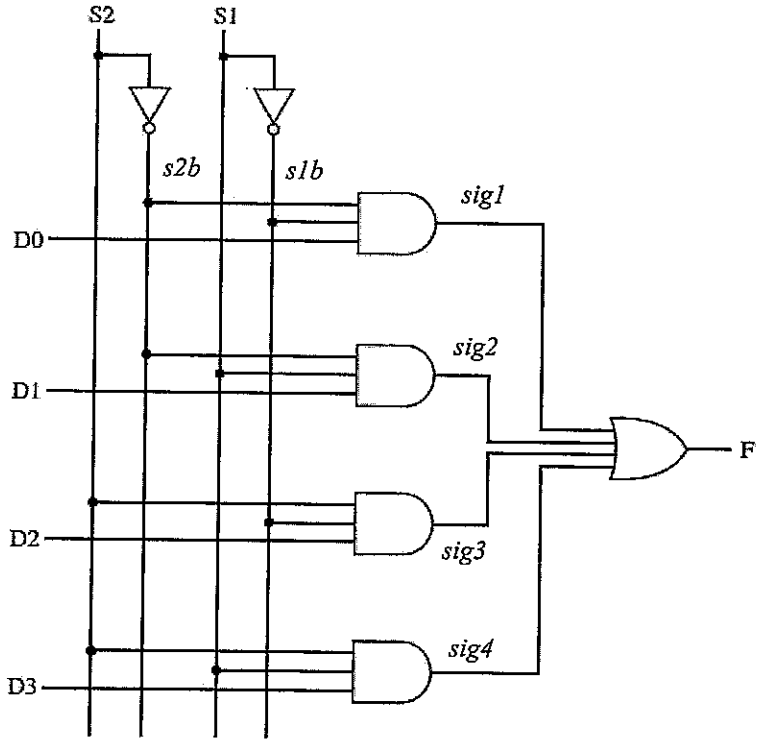

Figure Q1

Continued ...

Question 2

(a) Create the entity of the 3-bit Binary to Gray code decoder (Figure Q2) in VHDL. Use the entity name: *gray3*.

[3 marks]

Table Q2

Binary code B	Gray code G
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

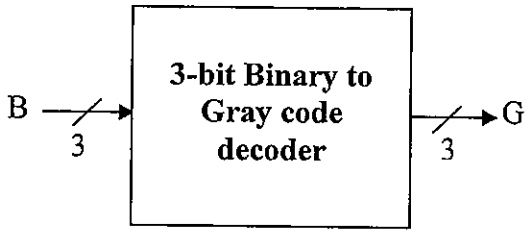

Figure Q2

(b) Design the ***architecture*** VHDL code for the 3-bit Binary to Gray code decoder (Figure Q2) using the following styles. Use the architecture name: *gray3_arch*. The truth table of the 3-bit Binary to Gray code decoder is shown in Table Q2.

(i) IF construct
(ii) Selected signal assignment
(iii) Conditional signal assignment

[8+7+7 marks]

Continued ...

Question 3

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity decoder2 is
 port(a : in STD_LOGIC_VECTOR(1 downto 0);
 b : out STD_LOGIC_VECTOR(3 downto 0));
end decoder2;

architecture arch of decoder2 is
begin

b(0) <= not a(0) and not a(1);
b(1) <= a(0) and not a(1);
b(2) <= not a(0) and a(1);
b(3) <= a(0) and a(1);

end arch;
```

Figure Q3

(a) Create a test-bench in VHDL code to test the system in Figure Q3, by referring to the *work.decoder2(arch)*. The time step for the test-bench is 100ns.

[13 marks]

(b) Create the truth table for the system in Figure Q3.

[4 marks]

(c) Sketch a waveform diagram to represent the test-bench signals created in part (a), and include the expected output in your waveform.

[4 marks]

(d) Synthesize the system in Figure Q3 using the standard logic gates.

[4 marks]

Continued ...

Question 4

(a) Create the VHDL code for the finite state machine shown in Figure Q4.
[17 marks]

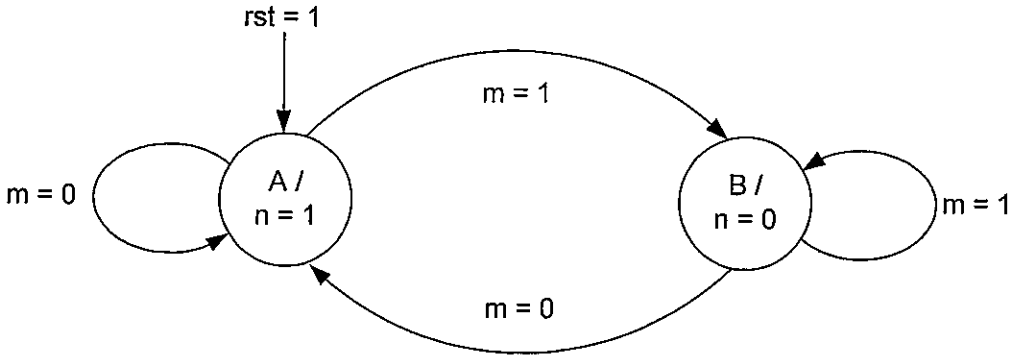

Figure Q4

(b) Modify and sketch the finite state machine in Figure Q4 using Mealy model.
[4 marks]

(c) Create the state table for the finite state machine shown in Figure Q4.
[4 marks]

End of Paper